

## EXCIMER LASER ANNEALING OF SILICON FILMS

S. Friligkos, M. Miyasaka<sup>1</sup>, J. Stoemenos

Department of Physics, Aristotle University of Thessaloniki, 54006 Thessaloniki, Greece

<sup>1</sup>Seiko Epson Corporation, Base Technology Research Center, Owa 3-3-5, Suwa, Nagano 392-8502, Japan

### Abstract

Amorphous silicon layers 50 nm thick were crystallized into polysilicon films by: a) excimer laser annealing (ELA), and b) a combination of solid phase crystallization (SPC) and subsequent ELA. Thin film transistors (TFTs) were then formed on fused quartz glass by a standard low temperature process ( $T < 600^\circ\text{C}$ ). The performance of the two groups of the resultant TFTs was compared. Their electrical properties were studied in correlation with the structural characteristics of the active polysilicon layers using transmission electron microscopy (TEM) and x-ray diffraction. The SPC films consist of large but heavily defected grains, the defects being mainly microtwins. These defects can be eliminated by the combination of melting and solidification taking place during the ELA process, when the laser energy density (LED) is between 280 and 360  $\text{mJcm}^{-2}$ .

### 1. Introduction

Poly-Si Thin Film Transistors (TFTs) are devices of considerable importance in the field of microelectronics. They are currently used as the key-devices for on-chip driver circuits in liquid crystal displays (LCDs) [1,2]. They are also potentially useful for the on-glass matrices of the LCDs used in high definition television receivers [3]. The most important step in the TFT fabrication process of the fully integrated LCDs is the growth of the active poly-Si film. Various methods of forming polysilicon layers on glass substrates have been reported up to now. A combination of low temperature SPC and ELA processes seems to be very promising since the poly-Si layer can be heated up to its melting temperature whereas thermal damage is not introduced into the underlying glass substrate. Moreover the crystalline grains of the polysilicon films thus formed are essentially defect-free [4]. This paper is focused on the structural characteristics of poly-Si films obtained by the two-step SPC and ELA process. The relationship between the physical properties of the poly-Si films and the electrical properties of the corresponding TFTs will be determined. The possibility to replace the single crystalline Si in SOI by polycrystalline Si fabricated on low cost glass and the realization of single grain thin film transistors will be shown.

### 2. Experimental procedure

Polysilicon films 50 nm thick were formed on glass substrates by use of the ELA (group A) and the combined SPC-ELA (group B) process. A 200 nm thick silicon oxide film was deposited on the substrate by electron cyclotron resonance plasma enhanced chemical vapour deposition method (ECR-PECVD). The precursor amorphous layers were deposited on top of the oxide film by the low pressure chemical vapour deposition (LPCVD) of disilane ( $\text{Si}_2\text{H}_6$ ), at  $425^\circ\text{C}$  and total pressure of 1.1 Torr. The group A amorphous films were subsequently annealed in a nitrogen ambient at  $425^\circ\text{C}$  for 2h. The group B films were annealed in a nitrogen ambient at  $600^\circ\text{C}$  for 24h and during this stage they were transformed into polycrystalline films. All specimens were then irradiated by KrF excimer laser light ( $\lambda = 248 \text{ nm}$ ) at room temperature. The duration of the laser pulse was 35 ns and its repetition rate 100 Hz. An optical homogenizer formed a uniform  $0,2 \times 300 \text{ mm}^2$  line-shaped profile.

Following the patterning of the polysilicon film a 120 nm-thick silicon dioxide ( $\text{SiO}_2$ ) gate insulator film was formed by ECR-PECVD at  $100^\circ\text{C}$ . A tantalum (Ta) film 750 nm thick was deposited by sputtering at  $150^\circ\text{C}$  and was suitably patterned to form the gate electrodes. Phosphine ( $\text{PH}_3$ ) and diborane ( $\text{B}_2\text{H}_6$ ) ions were used for the ion-implantation step at  $300^\circ\text{C}$ , the gate electrodes

playing the role of implantation masks leading to the formation of self-aligned NMOS and PMOS TFTs. An annealing step at 300°C for 3h in a forming gas ambient (3% hydrogen and 97% argon) was used for the activation of the implanted ions. The poly-Si films were characterized by combined cross-section TEM (XTEM) and planar view TEM (PVTEM).

### 3. Results and discussion

The films of group A, subjected only to ELA process, irradiated with Laser Energy Densities (LED) in the range 210 to 280 mJcm<sup>-2</sup>. The corresponding range for the mean grain size was from 67 to 145 nm respectively. The films irradiated with very low LED (210 mJcm<sup>-2</sup>) are microcrystalline with very smooth surfaces. In this case LED was not sufficient to cause melting of a significant portion of the film. The initially amorphous film undergoes an explosive solid state transformation into a fine-grained polycrystalline layer, as indicated by the grain size measured. As the LED increases the mean grain size also increases whereas the film surface becomes rougher. In the medium LED regime the film is melted throughout almost all its depth [5]. Only a very thin layer near the film-substrate interface remains solid. This layer can act as seed during the subsequent solidification leading to the formation of a polysilicon film with columnar grains. The last specimen of group A was irradiated with LED of 280 mJcm<sup>-2</sup>. Large hillocks are evident in the XTEM micrograph of fig. 1a. Significant mass transport has taken place in the grain boundaries and in the areas where planar defects were in contact with the film surface (denoted by arrows). The mean grain size is 145 nm as shown in the plane-view TEM micrograph of fig. 1b. In this case the LED used was sufficient to melt the film completely, leaving only a few Si islands unmelted. These islands can act as nucleation centers during the subsequent solidification process and thus lead to the formation of a poly-Si film with large grains [6]. Irradiation with higher LEDs leads to the complete melting of the amorphous film, the subsequent spontaneous nucleation in the melt and the final formation of a poly-Si layer with very smaller grains [7].

The structural characteristics of the a-Si film subjected only to SPC are shown in fig. 2. It is evident that the SPC process leads to the formation of large but heavily defected grains. The mean grain size calculated from the XTEM micrograph of fig. 2a was 2.5 μm. From the micrographs of figs. 2b and 2c (high magnification) it is evident that the density of the in-grain microtwins is of the order of 10<sup>12</sup> cm<sup>-2</sup>. It is known that microtwins in poly-Si are unstable and can be eliminated in temperatures higher than 750°C [8]. Thus a two-step annealing process beginning with a low-temperature thermal treatment at 600°C (formation of large but heavily defected grains) and going on with laser annealing with sufficient LED (elimination of microtwins), results in poly-Si films with good electrical characteristics.

In the micrographs of fig. 3 the structure of a specimen of group B irradiated with LED of 320 mJcm<sup>-2</sup> can be observed. From the XTEM micrograph of fig. 3a it can be seen that the in-grain twin density is reduced to an order of magnitude of 10<sup>8</sup> cm<sup>-2</sup>. On the other hand the plain-view micrograph of fig. 3b reveals well crystallized grains of the same size as the grains of the SPC film of fig. 2a. According to heat-flow simulations for the elimination of the in-grain defects at least 80% of the film must be melted [7]. Actually this is the case for the SPC+ELA film shown in fig. 3. Finally the group B specimen irradiated with LED of 340 mJcm<sup>-2</sup> was completely melted. In this case grains of different sizes coexist (smaller mean size 100 nm) and this fact indicates that superlateral growth took place. On the other hand LEDs lower than 320 mJcm<sup>-2</sup> were not sufficient to raise the temperature in the unmelted part of the films in order to annihilate the pre-existing microtwins. The above observations are in perfect agreement with the XRD results shown in fig. 4. An abrupt increase of the total XRD intensity can be observed for the SPC+ELA film irradiated with LED 320 mJcm<sup>-2</sup> and this also indicates the elimination of the in-grain defects. The abrupt decrease for LED 340 mJcm<sup>-2</sup> is due to the complete melting of the film and is accompanied by a similar decrease in grain size.

Mobility for the NMOS and PMOS devices of both groups were measured as a function of LED. The trend of the values observed is the same for NMOS and PMOS devices. From fig. 5 it is evident that NMOS TFTs fabricated on poly-Si films of group B have larger mobility. The best performance was shown by the TFTs formed on the film of group B irradiated with LED 320 mJcm<sup>-2</sup>, which for NMOS and PMOS are 155.2 and 69.1 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> respectively. The best TFTs of group A were these on films irradiated with LED 270 mJcm<sup>-2</sup>, NMOS 51.1 and PMOS 32.7 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> respectively.

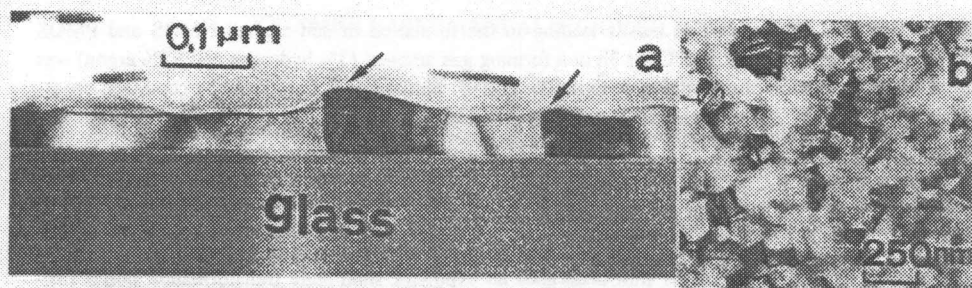


Fig.1 Group A-specimen irradiated with LED  $280 \text{ mJcm}^{-2}$ : a) XTEM micrograph hillocks denoted by arrows, b) plain-view micrograph (mean grain size 145 nm).

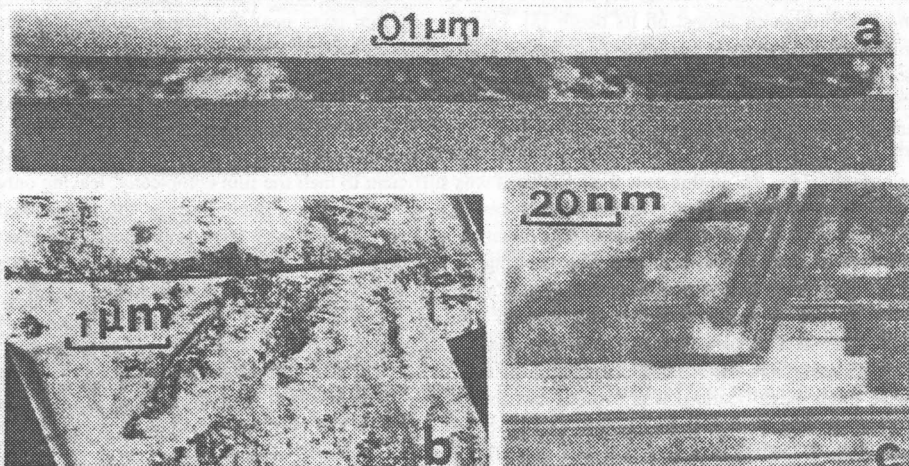


Fig.2 SPC film 50 nm thick: a) XTEM micrograph (surface very smooth), b) plane-view micrograph, c) plain-view micrograph at high magnification.

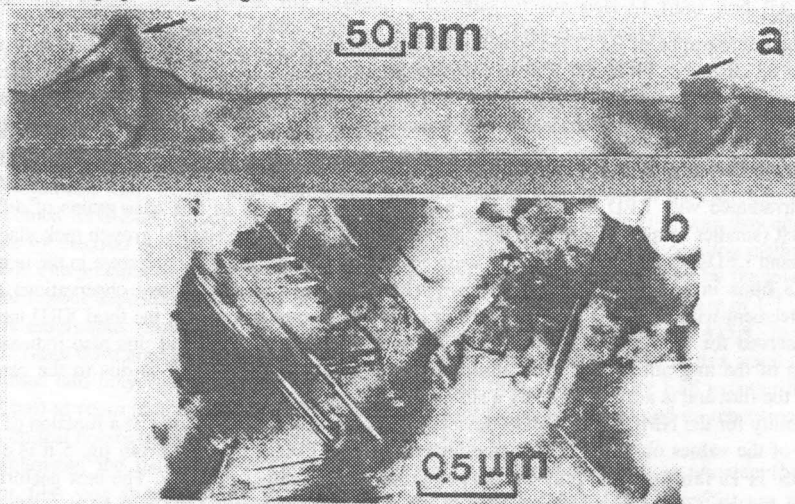


Fig.3 Group B specimen irradiated with LED  $320 \text{ mJcm}^{-2}$ : a) XTEM micrograph (hillocks at grain boundaries denoted by arrows), b) plain-view micrograph.

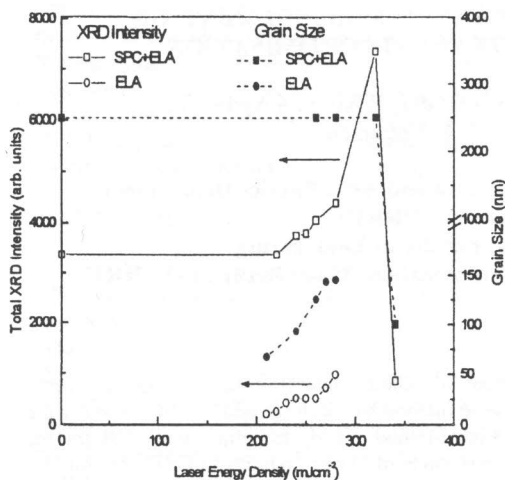


Fig.4 XRD intensity and grain size versus LED

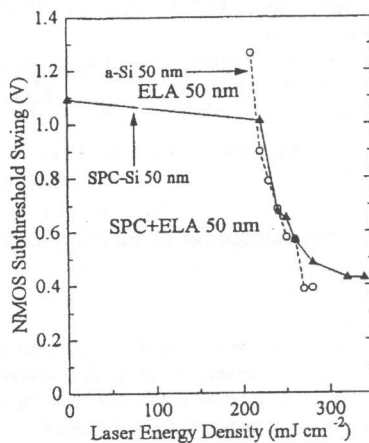


Fig.5 Mobility of NMOS TFTs versus LED.

From fig. 5 it is observed that for TFTs of group B the mobility increases as the LED increases up to the critical value, which corresponds to the complete melting of the film. From this point on poly-Si films with small grains are formed and the resultant TFTs exhibit considerably lower mobility values.

#### 4. Conclusion

The poly-Si TFTs fabricated on 50 nm-thick SPC+ELA films exhibit higher mobility values compared to those of a-Si+ELA films of the same thickness. This is attributed to the large grain size achieved by the SPC process and the elimination of the in-grain defects achieved by the ELA process. The ELA effectively reduces in-grain defects without affecting the crystalline grain size. As a result the combination of SPC+ELA processes results in a significant increase of the field effect mobility of the resultant TFTs. The above two-stage process is fully compatible with the soft glass substrates used today for flat panel displays and other videographic applications.

#### References

- [1] T. Sameshima, S. Usui and M. Sekiya, IEEE Electron Device Lett. **EDL** - 7 (1986) 276.
- [2] K. Sera, F. Okumura, H. Uchida, S. Itoh, S. Kaneko and K. Hotta, IEEE Trans. Electron Devices Lett. **ED** - 36 (1989) 2868.
- [3] H. Kuriyama, S. Kiyama, S. Noguchi, T. Kuwahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, H. Kawata, M. Osumi, S. Tsuda, S. Nakano and Y. Kuwano, Jpn. J. Appl. Phys. **30** (1991) 3700.
- [4] H. Kuriyama, T. Kuwahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, S. Noguchi, S. Kiyama, S. Tsuda, S. Nakano, M. Osumi and Y. Kuwano, MRS Bulletin, **31** (1992) 4550.
- [5] M. Miyasaka, J. Stoemenos, J. Appl. Phys. **86** (1999) 5556.
- [6] J. S. Im, H. J. Kim and M. O. Thompson, Appl. Phys. Lett. **63** (1993) 1969.
- [7] S. Friligkos, V. Papaioannou, J. Stoemenos, R. Carluccio, S. Cina, G. Fortunato, J. Cryst. Growth **182** (1997) 341.
- [8] L. Haji, P. Joubert, J. Stoemenos and N. Economou, J. Appl. Phys. **75** (1994) 3944